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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,858	06/20/2001	Hirokazu Sakaguchi	9319S-000226	4104

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,858	SAKAGUCHI, HIROKAZU	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 23, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frye et al. (US 5,534,465) in view of .

In re claim 1, Frye et al. shows (figs. 2 and 4) and LCD driver IC chip comprising a pad member (34) connected to an internal semiconductor device circuit (21) (see connection via below the pad into the n+ region) and having an electrical connection region to the exterior. At least one insulating film (35) is formed at a peripheral portion of the pad member and around the electrical connection region. A metal layer (36) covers the pad member and the insulating film. Figure 4 shows in another view that a bump electrode (41) is provided on the metal layer, wherein the bump electrode and the pad member lie above at least part of the semiconductor device circuit with an insulating interlayer (26) provided therebetween. Frye et al. shows all of the elements of the claims except the plurality of transistors. It would have been obvious to one of ordinary skill in the art to use two, three, four, etc., transistors since it has been held that mere

duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).* See also MPEP 2144.04 VI. (B). However, Kuroda et al. shows (fig. 47) a semiconductor device a bond pad (22) for a solder bump that is formed over and connect to a plurality of transistors (Qp and Qn). With this configuration, the size of the semiconductor can be decreased or the integration of the device can be improved (col. 4, lines 8-17). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the IC chip of Frye by forming a plurality of transistors under the pad and bump as taught by Kuroda to decrease the size of the chip and improve the device integration.

In re claim 2, Frye et al. shows (figs. 2 and 4) an integrated circuit chip comprising a device circuit, a transistor (21) in the device circuit, a pad (34) positioned above the transistor and connected to the device circuit (see connection via below the pad into the n+ region). An insulating interlayer (26) is formed between the pad and the transistor. Figure 4 shows in another view that a bump electrode (41) is on the pad. Frye et al. shows all of the elements of the claims except the plurality of transistors and the pad connected to each of them. It would have been obvious to one of ordinary skill in the art to use two, three, four, etc., transistors since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).* See also MPEP 2144.04 VI. (B). However, Kuroda et al. shows (fig. 47) a semiconductor device a bond pad (22) for a solder bump that is formed over and connect to a plurality of transistors (Qp and Qn).

With this configuration, the size of the semiconductor can be decreased or the integration of the device can be improved (col. 4, lines 8-17). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the IC chip of Frye by forming a plurality of transistors under the pad and bump as taught by Kuroda to decrease the size of the chip and improve the device integration.

In re claims 3 and 4, Frye inherently discloses that the circuit further comprises one of an input and output circuit because if the circuit is to be connected to the flip chip (40) as shown in figure 4, then the circuit must either receive input or provide output to that flip chip. In the same sense, the pad is either an input pad or an output pad.

In re claim 6, figure 2 of Frye shows that a via interconnects the pad (34) and the device circuit. The via is the portion under the pad (34) and connected to the contact on the n+ layer of the substrate.

In re claim 7, figure 2 of Frye shows that a lead layer (the contact layer on the n+ diffusion regions) of the insulating interlayer interconnects the via and the pad.

In re claim 8, figure 2 of Frye shows that a passivation film (35) is formed at a peripheral portion of the pad.

In re claim 9, figure 2 of Frye shows that a metal layer (36) covers the passivation film and the pad.

In re claim 10, figure 4 of Frye shows that the metal layer (36) is interposed between the pad (34) and the bump (41).

Response to Arguments

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Maeda et al. also shows forming a pad and bump electrode above a plurality of transistors to limit the amount cracks caused by stress.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

June 29, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800